REMARKS

Applicants have amended the Substitute Specification filed with the Preliminary Amendment submitted November 17, 2001, in order to correct a typographical error therein. Specifically, paragraph [0021] on page 8 of this Substitute Specification has been amended to provide proper dimensions for the sheet resistance of the metallic silicide layer. Noting, for example, original claim 57, as well as the paragraph bridging pages 8 and 9 of Applicant's original specification, clearly this amendment to the specification does not add new matter to the application.

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, each of the independent claims previously in the application (that is, claims 1, 8, 15, 22, 29, 36, 43, 50, 57 and 64) has been amended to recite that the step of sputter-etching sputter-etches away the top of the "semiconductor substrate" to 2.5 nm or less below the surface of the "semiconductor substrate". In addition, claims 2, 9, 16, 23, 30, 37, 44, 51, 58 and 65 have been cancelled without prejudice or disclaimer; and claims 3, 10, 17, 24, 31, 38, 45, 52, 59 and 66 have been amended to recite that the surface of the semiconductor substrate (rather than the surface of the source/drain regions) has been cleaned. Claims 7, 14, 21, 28, 35, 42, 49, 56, 63 and 70 have been amended to recite that the metal film forming step is performed under near-vacuum conditions, in the same apparatus in which the sputter-etching has been carried out. Claim 67 has been amended to be dependent on claim 64, rather than on claim 1; in light of this amendment of claim 67, it is respectfully submitted that the rejection of claim 67 under

the second paragraph of 35 USC §112, as being a duplicate of claim 4, has clearly been overcome.

Moreover, Applicants are adding new claims 71-112 to the application. Of these newly added claims, which are all directed to a method of fabricating a semiconductor integrated circuit device, claim 103 is the only independent claim, and will be discussed infra.

Of these newly added claims, claim 71 is dependent on claim 1, and recites that the source/drain regions formed on both sides of the gate electrode include first source/drain regions, and that the method includes the further steps of forming side walls on side surfaces of the gate electrode and forming second source/drain regions at sides of the side walls by injecting impurities into the semiconductor substrate, with these second source/drain regions having a higher impurity concentration than that of the first source/drain regions, the metal film being formed on the second source/drain regions. Claims 72 and 73, dependent respectively on claims 71 and 72, respectively recites that the metal film is formed in contact with the second source/drain regions and not in contact with the first source/drain regions; and recites that the metallic silicide layer is positioned such that current leakage between the metallic silicide layer and a junction formed by the first source/drain regions and the semiconductor substrate is prevented. Claims 76-102 recite subject matter expressly set forth in claims 71-73, but are dependent on independent claims previously considered by the Examiner. Claims 74 and 75, dependent respectively on claims 1 and 74, respectively recites thickness of the metallic silicide layer, and recites that the metal film is a cobalt film.

Independent claim 103 recites a method of fabricating a semiconductor integrated circuit device, including forming an insulating film on a semiconductor substrate, a conductive film on the insulating film and semiconductor regions in the semiconductor substrate self-aligned with the conductive film; and further recites sputter-etching away the top of the semiconductor substrate to 2.5 nm or less below the surface of the substrate, and forming silicide layers in the surface of the semiconductor regions and the conductive film. Claim 104, dependent on claim 103, recites that the semiconductor regions (set forth in claim 103) include first semiconductor regions and that the insulating film is a first insulating film; and recites additional steps, between the step of forming semiconductor regions and sputter-etching, of forming second insulating films on side surfaces of the conductive film and forming second semiconductor regions, having a greater impurity concentration than that of the first semiconductor region, in the semiconductor substrate, self-aligned with the second insulating film. Claim 104 further recites that the silicide layers are formed in the surface of the second semiconductor regions and the conductive film.
Claim 105, dependent on claim 104, recites that the silicide layers are not in contact with the first semiconductor regions; and claim 106, dependent on claim 105, recites that the silicide layers are positioned such that current leakage between the silicide layers and junctions formed by the first semiconductor region and semiconductor substrate is prevented. Claims 107 and 108 are each dependent on claim 103, and respectively recites that the sputter-etching is carried out after the surface of the semiconductor substrate has been cleaned; and recites that the sputter-etching is Ar sputter-etching. Claims 109 and 110, each dependent on claim 103, respectively

recites that the silicide layers are cobalt silicide layers, and recites that the cobalt silicide layers in the surface of the semiconductor regions have a thickness of 20-40 nm. Claims 111 and 112, dependent respectively on claims 103 and 111, respectively recites sputter-etching of the conductive film to a maximum depth of 2.5 nm, and recites that sputter-etching of the substrate and conductive film are performed simultaneously. See, e.g., paragraph [0069] on page 26 of Applicants' Substitute Specification.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in the Office Action mailed June 20, 2003, that is, the teachings of the U.S. patents to Kamal, et al., No. 6,303,503, to Zeininger, et al., No. 5,344,793, and to Matsubara, No. 6,096,638, and the pertinent pages of the publication by Wolf, Silicon Processing for the VLSI Era, Vol. 2 (1990), pages 150-2, under the provisions of 35 USC §102 and 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claims, having a standby current of 5 μA or less in tests of operation at 90°, or that is battery driven, and including the self-alignment technique forming the silicide layers, and wherein the top of the semiconductor substrate is sputter-etched away to 2.5 nm or less below the surface of the semiconductor substrate, with a metal film being formed on the source/drain regions and a metallic silicide layer being formed where the source/drain

regions are in contact with the metal film. Note each of independent claims 1, 8, 15, 22, 29, 36, 43, 50, 57 and 64.

More generally, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a method of fabricating a semiconductor integrated circuit device, including forming semiconductor regions self-aligned with a conductive film and forming silicide layers in the surface of the semiconductor regions and the conductive film, and including wherein the top of the semiconductor substrate is sputter-etched to 2.5 nm or less below the surface of the semiconductor substrate. See claim 103.

Moreover, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claims, having the step of sputter-etching as discussed previously with the forming of the silicide layers, and wherein the method includes further steps of forming side walls on side surfaces of the gate electrode and forming additional source/drain regions at sides of the side walls, these additional source/drain regions having a higher impurity concentration than that of first source/drain regions formed on both sides of the gate electrode, and wherein the metal film is formed on the second source/drain regions. Note claims 71, 76, 79, 82, 85, 88, 91, 94, 97 and 100; see also claim 104.

Furthermore, it is respectfully submitted that the teachings of the applied prior art would have neither disclosed nor would have suggested such method as discussed previously, having the feature of the sputter-etching and forming of the self-aligned metallic silicide, especially wherein the device formed has a standby current of 5 μA or

below in tests of operation at 90°C, and further wherein the metallic silicide layer has a thickness of 20 - 40 nm where the source/drain regions are in contact with the metallic film (see, e.g., claims 43 and 50; with respect to the thickness, see also claims 74 and 110); and/or wherein the gate electrode has a width of 0.18 μm or less, and the metallic silicide layer is formed with sheet resistance of 5 Ω/□ to 12 Ω/□ (see, e.g., claims 57 and 64).

Furthermore, it is respectfully submitted that these references as applied by the Examiner would have neither disclosed nor would have suggested the other aspects as in the present invention, as set forth in the remaining claims, having the feature of the sputter-etching and of forming the metallic silicide layer, and further including (but not limited to) wherein the sputter-etching is carried out after the surface of the semiconductor substrate has been cleaned by using hydrofluoric acid as a cleaning agent (note, for example, claim 3); and/or wherein the metal film forming step is performed under near-vacuum conditions, in the same apparatus in which the sputter-etching has been carried out (note, for example, claim 7); and/or the depth of sputter-etching of the conductive film (see claim 111), especially where the substrate and conductive film are simultaneously sputter-etched (see claim 112).

In any event, even assuming, arguendo, that the teachings of the applied prior art would have established a prima facie case of obviousness, the evidence of record in Applicants' disclosure, and in particular Fig. 9 and the description in connection therewith in paragraphs [0049] - [0051] on pages 20 and 21 of Applicants' Substitute Specification, together with Figs. 10-13 and the description in connection therewith in paragraphs [0054] - [0056] on pages 21-23 of Applicants' Substitute Specification,

show unexpectedly better results achieved according to the present invention, wherein the sputter-etching etches away only 2.5 nm or less below the surface of the semiconductor substrate, overcomes any prima facie case of obviousness, and clearly establishes patentability of the presently claimed subject matter. In this regard, it is respectfully submitted that this evidence in Applicants' specification must be considered in determining patentability of the present invention. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984),

The present invention as claimed in the above-identified application is directed to a technique for forming a semiconductor integrated circuit device, particularly effective for application to semiconductor integrated circuit devices with low levels of current consumption, and especially to devices such as a SRAM (static random access memory).

In forming SRAMs, a silicide layer has been formed on the source/drain regions of MISFETs of the memory, to decrease resistance of the source/drain region and to decrease the contact resistance between the source/drain and a plug that is subsequently to be formed on the source/drain region. The silicide layer is formed by depositing a metal layer on the source/drain region and on the gate electrode, and then causing silicidation in the part where the source/region (silicon substrate) and a metal layer come into contact, and in the part where the gate electrode (silicon layer) and the metal layer come into contact.

However, with the miniaturization that accompanies an increase in the degree of integration of memory cells, gate widths decrease and junction depths of source/drain regions become shallow. Moreover, it is desired to reduce power consumption,

particularly in mobile products such as cellular phones and notebook-sized personal computers, which are driven by batteries.

In miniaturized devices, particularly in low power consumption devices, utilizing a conventional technique of forming the silicide wherein approximately 3 nm to 5 nm is etched away from the surface of the silicon substrate and then layers are deposited and thermally processed to form the silicide layer, various problems arise. In particular, formation of a deep layer silicide on the source/drain regions increase current leakage between the source/drain regions and the semiconductor substrate. As a result, the current when standing by exceeds a critical value, and thus reduces the yield of the products. In addition, even when the standby current is less than a critical value, the time over which it is possible to use a battery-driven mobile product is shortened by the inclusion of a semiconductor integrated circuit device that has a relatively large standby current.

Against this background, Applicants provide a method of fabricating a semiconductor integrated circuit device, for example, that has a standby current of 5 μA or below in tests of operation at 90°C, having improved yield and reduced power consumption; and, in particular, can avoid the aforementioned current leakage. Applicants have found that by sputter-etching away the top of the semiconductor substrate at most 2.5 nm below the surface of the substrate (that is, sputter-etching the semiconductor substrate to a depth of at most 2.5 nm), the aforementioned current leakage can be avoided, and yield improved and power consumption reduced, even in large integration and with a semiconductor integrated circuit device that has a standby current of 5 μA or below in tests of operation at 90°C.

In addition, by carrying out the etching and metal forming step in the same apparatus, the metal forming step being performed under near-vacuum conditions, the introduction of an oxide film prior to forming the metal film can be avoided.

As for the unexpectedly better advantages achieved with an amount of sputter-etching of 2.5 nm or less, as in the present claims, attention is respectfully directed to Fig. 9 and the description in connection therewith in paragraphs [0049] - [0053] on pages 21 and 22 of Applicants' Substitute Specification. Noting particularly line (b), a standby current of 5μA or below, it can easily be seen that the yield is improved when the amount of sputter-etching is 1 or 2 nm as compared with the case where no sputter-etching is carried out or where an amount of sputter-etching is 3 or 4 nm. Particularly where the amount of sputter-etching is 3 or 4 nm, the yield becomes lower than in the case where no sputter-etching is carried out, when the critical value of the standby current (Isb) is set to 5 μA or below.

Attention is also respectfully directed to Figs. 10-13 and the corresponding descriptions in connection therewith in paragraphs [0054] - [0056] on pages 22-24 of Applicants' Substitute Specification. As seen particularly in Figs. 11 and 12, as compared with Fig. 13, the greater the amount of sputter-etching, the greater the number of chips with large flows of standby current. As can be appreciated, the smaller the standby current, the better the performance of the chip. Thus, as can be appreciated from the experimental data in Applicants' Substitute Specification, when the amount of sputter-etching is set to 2.5 nm or less, more chips with lower levels of standby current can be obtained, so that more chips with high levels of performance can be obtained. Thus, it is possible to reduce the standby current of the

semiconductor integrated circuit device and to reduce its consumption of current. As a result, semiconductor integrated circuit devices formed by the present method are applicable in cellular phones and personal computers which are battery-driven, as they are able to lengthen the times over which these products are used.

Attention is also directed to Fig. 15 of the above-identified application, and the description in connection therewith in paragraph [0064] on pages 25 and 26 of Applicants' Substitute Specification. As is clear therefrom, where the sputter-etching is undesirably great, for example, greater than 2.5 nm, upon forming the silicide the metal silicide layer approaches the junctions of the source/drain regions, increasing the current leakage. This is avoided according to the present invention; having the sputter-etching to a depth of at most 2.5 nm, such approach to the junction, and resulting increase in the current leakage, can be avoided.

In addition, by etching the surface of the gate electrode to a relatively small thickness, a discontinuity of the layer of metallic silicide can be avoided, so that increase of resistance of the gate electrode layer, and a resulting decrease in operation speed, can be avoided. Note paragraphs [0067] - [0069] on pages 26-28 of Applicants' Substitute Specification. See claims 111 and 112.

Kamal, et al., discloses processes for the formation of cobalt salicide layers, during semiconductor device fabrication, including a sputter etch surface preparation step prior to a cobalt layer deposition step. This patent discloses that the surface of the MOS transistor structure is prepared using an argon sputter etch process with a DC bias of less than -280 volts, the argon sputter etch process conditions being optimized in order to minimize the backsputtering of silicon onto the gate sidewall spacers, while

still adequately removing native silicon dioxide from the source region, drain region and silicon region. See column 1, lines 8-12; note also column 2, lines 48-55 and 58-66. This patent discloses that following the argon sputter etch process step, a cobalt layer is deposited on the source region, drain region, silicon gate and gate sidewall spacers; and cobalt in the cobalt layer that is in contact with silicon from the source region, drain region and silicon gate is then reacted to form self-aligned cobalt silicide layers thereon. See column 3, lines 9-15. This patent goes on to state that particularly useful "soft" argon sputter etch processes are those having native silicon dioxide etch rates ranging from 5 angstroms per second to less than 10 angstroms and with native silicon dioxide removal targets of between 20 and 60 angstroms. Note column 5, lines 60-65.

Initially, it is respectfully submitted that Kamal, et al. is concerned with removing silicon oxide from the surface of the semiconductor substrate. It is respectfully submitted that this reference does not disclose, much less would have suggested, sputter-etching away the top of the semiconductor substrate, to 2.5 nm or less below the surface of the semiconductor substrate.

In addition, it is respectfully submitted that the teachings of Kamal, et al., directed to removal particularly of native silicon dioxide, would have neither taught nor would have suggested the problem arising in connection with etching to too great a depth of the silicon substrate, and avoidance of such problems by sputter etching to a depth of 2.5 nm or less below the surface of the semiconductor substrate.

Reference by the Examiner, in connection with the teachings of Kamal, et al., to removal of native oxide thickness of 20 angstroms, the Examiner contending that this meets the amount being sputter etched as in the present claims, is noted. See the first

full paragraph on page 3 of the Office Action mailed June 20, 2003. However, it is emphasized that the present claims recite sputter-etching away the top of the semiconductor substrate, to 2.5 nm or less below the surface of the semiconductor substrate. That is, it is respectfully submitted that according to the present invention a maximum amount of etching of the substrate, not of native oxide thickness, is recited. Even as Kamal, et al. is interpreted by the Examiner, of including removal of native oxide, it is respectfully submitted that this patent would have neither taught nor would have suggested the presently claimed subject matter, and advantages thereof.

It is again emphasized that according to the present invention, Applicants have found a source of the current leakage problem, and a technique to avoid this problem, by etching at most 2.5 nm of the semiconductor substrate from the surface thereof. Particularly in view of the problem addressed by the present invention, which is not addressed in Kamal, et al., and the solution thereto, providing unexpectedly better results as seen by the evidence in Applicants' disclosure, it is respectfully submitted that the presently claimed subject matter patentably distinguishes over the teachings of Kamal, et al.

It is respectfully submitted that the additional teachings of the Zeininger, et al. would not have rectified the deficiencies of Kamal, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art. Zeininger, et al. discloses a method of forming semiconductor integrated circuit devices having silicided junctions. According to one described aspect in this patent, a silicon wafer is first precleaned with hydrofluoric acid; and after the HF precleaning, the silicon wafer is transferred to a conventional cobalt sputtering tool where it is sputter

cleaned by bombardment with low energy ions. The low energy bombardment forms an ultra-shallow damage region in the bulk silicon; and after the sputter cleaning, cobalt metal is deposited on the silicon wafer at room temperature so as to form a $CoSi_2$ layer. Note particularly column 1, line 60 to column 2, line 3. See also column 2, lines 39-42 and 68-64. Note also column 3, lines 6-9, disclosing that cobalt metal is deposited on the wafers using the same cobalt sputtering tool in which the wafers were sputter cleaned.

Initially, it is noted that Zeininger, et al. discloses sputter cleaning, not sputter etching. It is respectfully submitted that one of ordinary skill in the art as described in Kamal, et al., disclosing sputter etching of native silicon dioxide and thereafter a cobalt layer deposition, would not have looked to the sputter cleaning of Zeininger, et al.

In any event, even assuming the teachings of Kamal, et al. and Zeininger, et al. were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including the maximum sputter etching, and unexpectedly better advantages achieved thereby, as discussed in the foregoing.

Matsubara discloses a method for forming a refractory metal silicide layer on a silicon surface, in which a first layer made of a refractory metal is formed on the silicon surface, and a second layer is formed which extends over the first layer. The second layer may be made of the same refractory metal as the first layer, and contains nitrogen, wherein a ratio in composition of nitrogen to the refractory metal is less than 1:1. The silicon surface and the first and second layers are then subjected to a heat treatment in a nitrogen free atmosphere having a pressure of not less than ultra high

vacuum to form a refractory metal silicide layer on an interface between the silicon surface and the first layer. Note column 8, lines 8-10. See also column 10, lines 1-11; column 11, lines 48-50; column 12, line 64 to column 13, line 4; and column 13, lines 40-55.

Wolf, as applied by the Examiner, discloses various silicide thicknesses.

Even assuming, arguendo, that the teachings of Matsubara and Wolf were properly combinable with the teachings of Kamal, et al. and of Zeininger, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed method, including the sputter-etching away the top of the semiconductor substrate to 2.5 nm or less below the surface of the semiconductor substrate and unexpectedly better results achieved thereby, or other aspects of the present invention as discussed in the foregoing.

Moreover, it is emphasized that problems in connection with the sputter etching are increased greatly with miniaturized devices (for example, gate widths of 0.18 μm or less); the present invention avoids previously discussed problems, even with such miniaturized devices. Particularly in view of the increased problems with large-scale devices, such increased problems even being avoided by the present invention, the present invention particularly patentably distinguishes over the teachings of the applied prior art.

In addition, the present invention provides advantages of reduced power consumption, for example, and improved speed, with silicide thickness or sheet resistance of the silicide as in the present claims. Such additional advantages

according to the present invention provide additional features further patentably distinguishing over the applied prior art.

The additional contention by the Examiner in the first paragraph on page 5 of the Office Action mailed June 20, 2003, that the optimization of the extent of the sputter etching would have been obvious, mainly, to form ultra-shallow damage region and to obviate disadvantages such as agglomeration, layer degradation and leaky junctions, is noted. The Examiner is respectfully requested to point out the specific portions of the references referring to, inter alia, leaky junctions. As can be seen in the evidence in Applicants' disclosure, it is respectfully submitted that the present invention, utilizing sputter etching of 2.5 nm or less below the surface of the semiconductor substrate, provides unexpectedly better results; and on this basis alone it is respectfully submitted that Applicants have clearly rebutted any conclusion by the Examiner that optimization of the extent of the sputter etching would have been obvious.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.40724X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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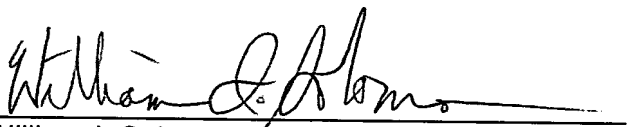

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